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UVM BASED VERIFICATION OF DUAL PORT SRAM BY IMPLEMENTING BIST

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ABSTRACT

In this paper, we present a coverage driven functional verification based on UVM methodology using system Verilog language. As transistor scaled down, memory area on-chip & density of memory drastically increases. Which leads to an exponential increase in the problem of faults in memory? So, we present Built-in self-test which is used to detect and repair the faults in multi-ported memory. This BIST is design based on DFT concepts which use MARCH C test algorithm. We used layered UVM test bench architecture which allows engineer work independently and simplifies verification process by code re-usability feature.

***KEYWORDS**: UVM (Universal Verification Methodology [9]), BIST (Built-In-Self-Test), Dual Port SRAM, Code Re-Usability, MARCH C*